

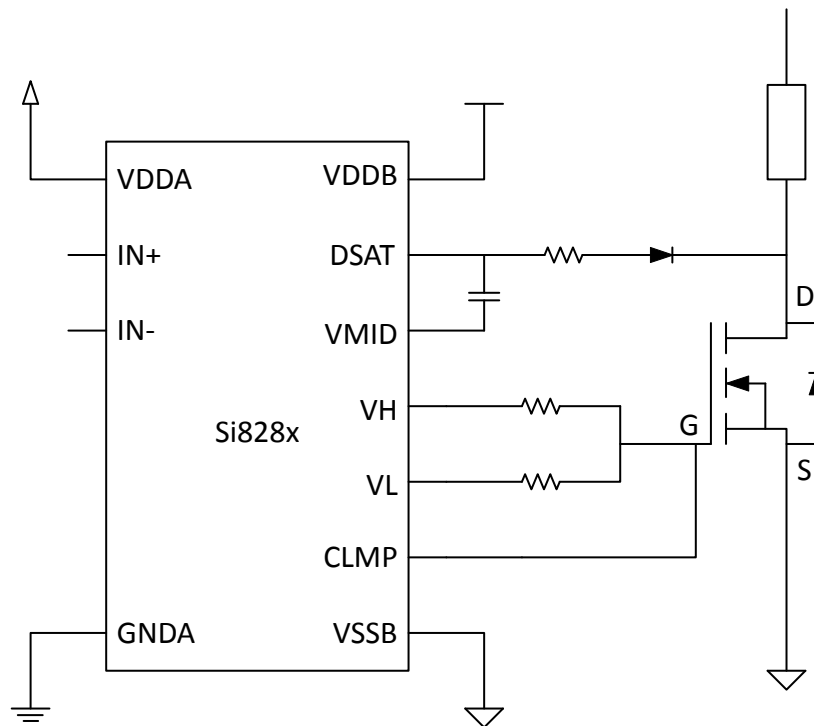
AN1306: Driving SiC MOSFET Switches Using the Si828x Isolated Gate Driver

The Si828x products integrate isolation, gate drivers, fault detection, MOSFET protection, and readiness indicators into one package to drive power switch devices. The Si828x family can optimally drive SiC MOSFET switches in the most demanding applications through the addition of external circuits to boost gate drive current to the SiC MOSFET gate and fine-tune the DESAT protection, Soft Shutdown, and Miller voltage clamp.

This application note discusses drive requirements for SiC MOSFET switch devices. It provides guidance for selecting the external components necessary for driving and protecting SiC MOSFET switches in high-voltage, high-performance applications.

KEY FEATURES

- Describes how Si828x family can optimally drive SiC MOSFETs
- Provides guidance on circuit bill-of-materials for tuning desaturation detection timing, soft shutdown duration, and Miller voltage clamping
- Shows how to build a simple external boost circuit for decreasing switching time, and thereby reducing switching losses



1. Introduction

Silicon carbide (SiC) MOSFET power switches are appropriate for a wide variety of inverter and motor control applications. Their device characteristics provide the basis for many performance advantages over silicon MOSFETs and IGBTs. While they present a similar functional load to a gate driver, they are different from standard MOS or IGBT power switches in several ways that place special demands on gate drive circuits.

Designers may be motivated to choose SiC transistors over MOS or IGBT by factors such as lower switching losses, higher switching speeds, better thermal performance, higher power density, and lower system costs (despite the cost difference of the switch itself). For instance: for comparable devices operating at the same frequency, an IGBT circuit shows a 7X switching loss in contrast to a similar SiC device. To bring switching losses into near parity, the IGBT circuit must have its switching frequency reduced by 2/3. This results in an increased magnetics cost for the IGBT circuit of 2.5X, higher weight, and higher power loss. While SiC MOSFETs are currently more expensive than IGBTs (at time of publication, Q1 of 2021), as economies of scale kick in they will be lower in cost.

The Si828x family of Gate Driver ICs is easily adapted for use with SiC MOSFET power switches by using external bill-of-materials (BOM) enhancements, yielding excellent performance and safe operation. This application note provides details on SiC gate drive requirements and choosing external BOM components to obtain optimal performance in gate drive and power switch safety.

2. Silicon Carbide Device Characteristics

Silicon carbide is a wide bandgap semiconductor material. About three times the energy is required to move electrons from the valence band to the conduction band. As a result, silicon carbide has a high critical breakdown strength on the order of ten times that of silicon. SiC components may have blocking voltages that are an order of magnitude higher than those made of silicon. The high breakdown strength allows for a thinner device structure than silicon for a given breakdown voltage. The thinner device structure of silicon carbide allows reduction of on-resistance by some two orders of magnitude compared to silicon. As a function of temperature, SiC devices have a much more stable drain-to-source resistance, or R_{DS-ON} . Compared to silicon and gallium nitride, with R_{DS-ON} normalized to 1 at 25 °C, R_{DS-ON} for SiC is 1.3X at 175 °C, for silicon is 2.8X at 175 °C, and for gallium nitride is 3.0X at 175 °C. Silicon carbide also has a thermal conductivity 2.8X higher than silicon, allowing for a much higher current density at a given junction temperature than a comparable silicon device. The silicon carbide bandgap is approximately 3X wider than silicon. SiC devices thereby have more than two orders of magnitude lower leakage current at high temperature operation (~100 times less). For more information on this topic, see the articles, "[Silicon carbide MOSFETS](#)" and "[Application Considerations for Silicon Carbide MOSFETS](#)".

Whereas the IGBT has an exponential ID v. VDS curve with a conduction knee, the SiC has a linear ID versus VDS curve. At rated current the conduction losses may match but SiC conduction losses are lower at lower current. In fact, below 99% rated current, SiC conduction losses are lower than those of an IGBT.

Being a minority-carrier device, the IGBT must remove minority carriers from the N-drift region (gate) when it turns off. When the V_{CE} has risen to a point where the depletion region has expanded, the minority carriers participate in internal recombination current. This is called the tail current; it is the collector current when V_{CE} is high. This tail current contributes to switching loss. In contrast, the SiC transistor does not exhibit a tail current and thus has a much lower switching loss in a comparable device. Again, refer to the article, "[Application Considerations for Silicon Carbide MOSFETS](#)", for more information.

The SiC body diode exists in a majority carrier environment. This, in combination with a thinner N- layer, results in fewer minority carriers to be swept out of the N- layer during recovery, which takes much less time than sweeping out the minority carriers present in the thick IGBT N- layer. A very short SiC diode recovery time results in a very fast switching time. Fast switching time reduces the ringing time. The combination of no tail current and fast body diode recovery means that a SiC transistor has very high switching speeds relative to a comparable IGBT transistor.

To summarize, SiC transistors have lower conduction losses over the VDS range and lower switching losses. They have lower leakage at high temperatures. Their current density is higher. They have a resistance versus temperature curve that is much flatter. They are smaller and have a lower on-resistance for a given size die. They are thinner, resulting in better thermal performance. Their high breakdown voltages enable performance at much higher power conversion rates.

3. Device Characteristics Impact Driver Requirements

SiC MOSFETs are much like other power switches, and each places special demands on the drive circuit. The following sections discuss key device characteristics and how they impact driver design.

3.1 Low Transconductance Requires High ON-state Drive Voltage and May Require Negative OFF-state Drive Voltage

The SiC MOSFET has a relatively low transconductance as contrasted with silicon MOSFETs and IGBTs. This requires a higher gate-source voltage (V_{GS}) to cause the device to transition from OFF state through the linear region to full saturation quickly. Also helpful is a very fast transition of the gate voltage from low to high. This rapid but high voltage change on the gate and the resulting rapid conduction transition will minimize transition conduction losses.

Importantly, the low transconductance will also have an influence on desaturation detection circuits. A device with higher transconductance will enter saturation at a lower gate-source voltage, achieving its optimum $R_{DS(on)}$ more easily. By contrast, the SiC MOSFET will tend to remain in the ohmic or transition region over a broader range of V_{GS} , resulting in more opportunity to desaturate in an overload situation. This may require a reduction of the desaturation detection threshold to get safe operation during an overload. Fortunately, the low gate charge of the SiC in combination with high gate drive helps speed the transition from OFF to ON state, minimizing the time in the non-saturated state.

Hard-switched applications (hard-switched circuits have the output node switched between power supply rails) that have high switching rates will do well to use a negative gate supply for turn-off. The negative swing of the gate drive will help by maintaining a higher negative slew rate (therefore a shorter off-transition), and the negative gate voltage will provide some noise immunity from C_{DG} -conducted switching energy from the drain as the high-side device turns on.

3.2 High Gate Resistance Needs Low-Impedance Driver

Compared to silicon switching devices, SiC devices have higher internal gate resistances. This translates to the need for low-impedance drivers. A gate driver optimized for use with IGBTs will not have an output impedance low enough to properly drive the high gate resistance. The external drive enhancements discussed in this document solve the problem of driver output impedance.

3.3 Absence of Tail Current Requires Snubbers

The tail current of the IGBT results in slower turn-off, which also dampens parasitic effects during turn-off. The SiC device has effectively no tail current, but the more rapid turn-off of a hard-switched, low-side device may result in drain overshoot and more ringing due to parasitic inductive effects. This additional overshoot may cause damage to the device. This damage may be eliminated by designing snubber circuits to manage the parasitic effects and mitigate overshoot and circuit ringing.

3.4 High dv/dt Needs Positive and Negative Gate Drive

SiC devices require high dv/dt gate drive to take advantage of low gate charge and to bring the devices from OFF state to fully ON state most rapidly to prevent transition conduction losses. Such high slew rate gate drive signals can interact with parasitic inductances resulting in gate drive ringing. High drain dv/dt in H-bridge circuits can result in dynamic current through the drain-gate capacitance and the gate-source voltage may rise enough to turn the device on. Both effects can be mitigated by using a negative gate drive supply for turn-off, especially in hard-switched applications.

3.5 Lower Noise Margin Needs Noise Immunity Against Gate Drive Ringing

SiC MOSFET device operation benefits from a clean, square gate drive pulse, free of excessive ringing.

A SiC device may have a nominal threshold voltage of 2.3 V at which the device just begins to turn on, but not turn on fully until the gate-source voltage reaches 15 V or more. This causes the SiC MOSFET to have a lower noise margin than silicon devices. If gate drive resistance is carefully controlled, the gate drive pulse will be adequately dampened, and undesired turn-off or turn-on will be avoided.

The gate drive and its return path comprise a loop which will contain inductive parasitic elements. These elements will contribute to gate drive ringing. By minimizing this loop inductance, less gate drive resistance is required, and rise/fall times will be minimized. Make sure the gate drive is as close as possible to the SiC gate to minimize loop inductance.

The source lead of the SiC device will carry high switching currents at high di/dt . This will result in voltage drop across the parasitic source lead inductance. This may result in oscillation in the gate loop and effectively lower frequency response. Some SiC MOSFETs have a Kelvin connection for the gate drive return which takes the bulk of the source lead inductance out of the gate drive loop, mitigating loop oscillation and improving response.

3.6 High-Speed Operation Requires Noise Immunity Against dV/dt (Common Mode Transient Immunity)

Hard-switched SiC circuits are operated at high switching frequencies and at high voltages. The high dV/dt of the high-side source can result in a challenge to the common mode transient immunity (CMTI) of the driver isolation barrier (see application note, "[AN1167: Safety Considerations for Skyworks Series Capacitor Isolators](#)"). The barrier may see common mode transient dV/dt in excess of 100 kV/ μ s. These transient rates may impact the selection of the gate driver and may require more careful attention to the gate driver resistor values used for slowing down the gate drive rise and fall.

3.7 High-Voltage Operation Needs Adequate Working Insulation Voltage (VIOWM), Creepage, and Clearance

Isolated gate drivers must comply with certain safety specifications. High-voltage switching circuits are expected to work continuously over a long lifetime. This voltage relates to a driver specification called maximum working insulation voltage, or VIOWM. The possibility of much higher voltage exposure at some phase of operation requires the driver to comply with a specification called rated dielectric withstand voltage, which the device must withstand for 60 seconds in qualification. Safety requirements demand a certain minimum creepage distance to ensure against arcing across the isolation barrier. This distance is the shortest distance across the surface of the package from a primary side pin to a secondary side pin (see application note, "[AN583: Safety Considerations and Layout Recommendations for Digital Isolators](#)").

3.8 Fast Switching Times Require High Driving (Source/Sink) Capability

SiC MOSFET devices have much lower total gate charge than conventional silicon devices; however, due to their lower transconductance, the SiC devices require higher gate voltage swing than what silicon MOSFETs and IGBTs need. Even so, the product of gate voltage swing and gate charge is lower for a SiC than for a similar silicon or IGBT device. We wish to take advantage of this by using fast gate switching times, which requires high-drive capability to get the fastest possible gate dV/dt .

3.9 Low Deadtime Operation and Parallel Switches Need Low Propagation Delay and Channel Mismatch <10 ns

Hard-switched (e.g., half-bridge) applications must avoid shoot through currents. Thus, some deadtime during which both high-side and low-side switching devices are off must be designed into the control scheme. However, the dead time must be minimized to keep the efficiency gains of high switching frequencies. This translates into a requirement for low propagation delay in the gate driver.

Very large parallel device arrangements may require more than one gate driver to achieve desired performance. Each section must not only keep deadtime to a minimum, the matching of propagation delay between drivers must also be very tight to minimize system deadtime and maximize efficiency in such high-power applications.

4. Silicon Carbide MOSFET Gate Drive Models

4.1 Simple Driver Model

The figure below shows the simple driver with one output pin driving the gate of a MOSFET through the gate resistor R_g . Because both gate charging and discharging current levels are determined by R_g , the rise and fall times are the same. This driver model works well for applications where independent rise and fall times are not necessary and the Miller current generated by the dV/dt at the MOSFET drain terminal through the parasitic C_{GD} is small, hence a Miller clamp is not needed.

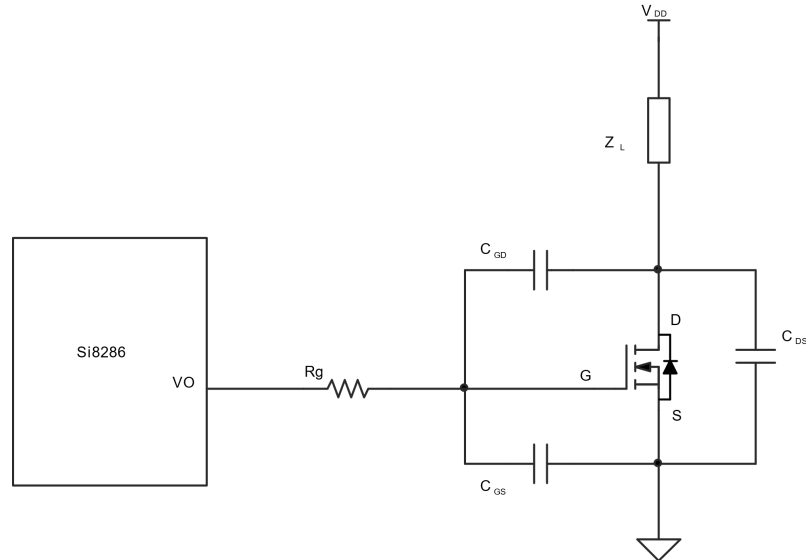


Figure 4.1. Simple Driver Model

4.2 Three Output Pin Driver

The figure below illustrates a driver with separated VH and VL (separate output high and output low) pins that allow independent setting of the switch's turn-on and turn-off times. This capability is quite helpful in half-bridge configuration ([Figure 7.2 Half-Bridge Circuit with Three-Output-Pins Driver on page 16](#)) where the speed of the turn-on and turn-off are aligned to minimize shoot-through current (see [Figure 7.4 Lower Shoot-Through Current, \$R_H \gg R_L\$ on page 17](#)). The low-impedance Miller clamping pin (CLMP) attenuates the Miller voltage spikes and renders the driver with three output pins more suitable for driving high power MOSFET/IGBT with larger input gate C_{GS} and C_{DS} capacitances.

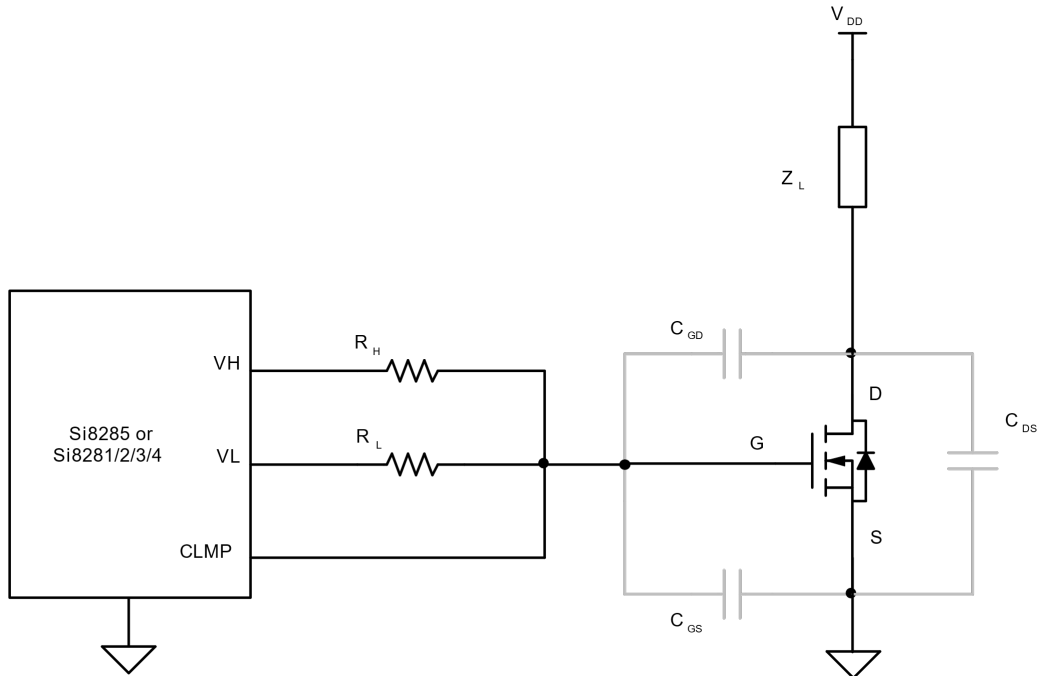


Figure 4.2. Driver Model with Three Output Pins

4.3 Simple Driver Model with Independent Rise and Fall Times

The following figure demonstrates an option for the Simple Driver circuit to achieve independent control of the rise and fall times by use of a steering diode. It is recommended to use 100 V, 1 A fast diode, like an ES1B diode, to ensure adequate turn-off speed and meet the operational voltage-current requirements of the driver circuit. Note that, because the turn-off current flows through both R_H and R_L , adjustment to the R_L value is required to ensure the desired turn-off transition time (see [7.2 Calculating \$R_H\$, \$R_L\$ Gate Resistors](#)).

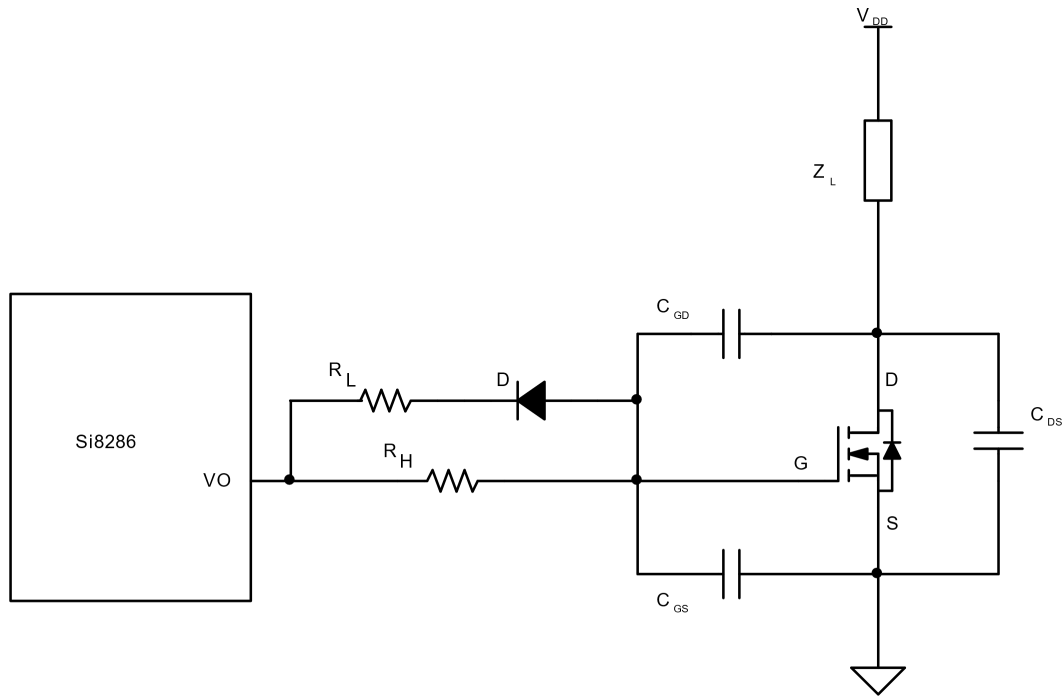


Figure 4.3. Simple Driver with Independent Rise and Fall Times

5. Si828x Gate Driver IC

5.1 Standard Features

The Si828x family of gate drivers have certain standard features which make them ideal for driving power MOSFETs and IGBTs used in a wide variety of inverter and motor control applications. These features include:

- 5.0 kVrms isolation per UL 1577
- High drive peak output current = 2.5 A minimum. Low drive peak output current = 3.0 A minimum
- DESAT detection
- Soft shutdown on fault condition
- Integrated Miller Clamp
- FAULT feedback
- Gate driver supply range from 9.5 V to 30 V
- Integrated dc-dc converter (Si8281/82/83/84)

However, a few external bill-of-materials enhancements make the Si828x an ideal solution for driving SiC MOSFET power switches in a safe, effective manner. These enhancements are presented briefly here and discussed in detail in application note, "[AN1288: Si828x External Enhancement Circuits](#)". These enhancements may be applied individually or in combination.

5.2 External Bill-of-Materials Enhancements

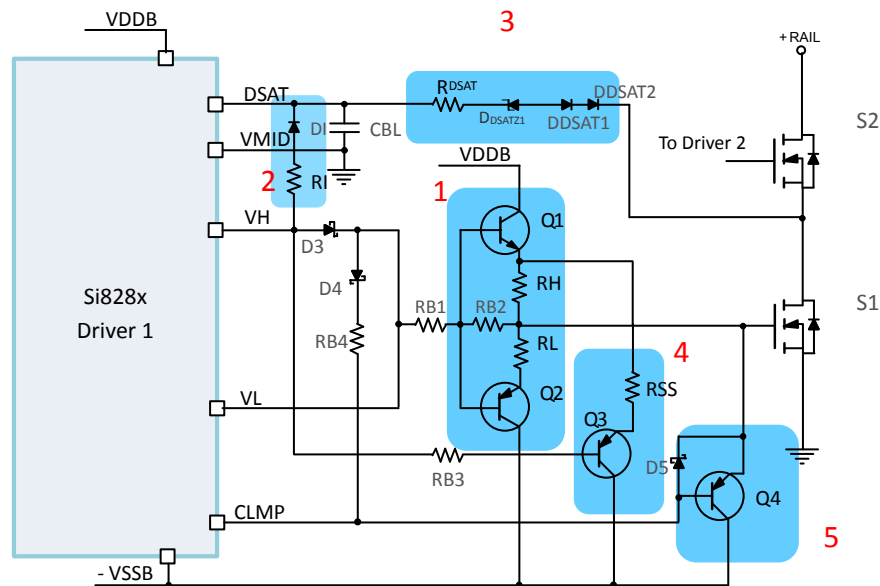


Figure 5.1. External Driver and Protection Enhancements

Refer to the figure above in the following sections.

5.2.1 Gate Drive

Transistors Q1 and Q2 provide enhanced gate drive current, increasing it from ± 3 A to ± 20 A and more, depending on the choice of PNP and NPN. These transistors source current from gate drive supplies ($V_{DDB} - V_{SSB}$) ranging from 9.5 V to 30 V, with negative supply ($V_{MID} - V_{SSB}$) range of 0 V to 15 V. Using these buffer transistors provides a greater drive current window, which can then be tuned with resistors RH and RL that serve to dampen the effects of parasitic inductances in the gate drive path and eliminate the occurrence of ringing-induced undesired turn-on or turn-off of the SiC MOSFET. This helps to reduce switching losses and eliminate shoot-through currents in half-bridge circuits.

5.2.2 DESAT Protection Response Time

DESAT protection response time has three components:

- t_{BLANKING} , or DESAT detection blanking time, during which DESAT detection is disabled.
- $t_{\text{DESAT to SS}}$, or $t_{\text{DESAT}(90\%)}$, the internal delay between DESAT detection and the beginning of soft shutdown.
- t_{SS} , or Soft Shutdown Time, during which the switch gate is pulled toward VSSB and reaches the Miller Clamp pin threshold voltage.

Optional components RI and DI come into play when VH is high, driving the gate high. They conduct current into the blanking capacitor. This current adds to I_{chg} and causes the DESAT threshold to be reached sooner during a desaturation event.

$T_{\text{DESAT to SS}}$ is an internal delay which is mostly independent of external factors.

5.2.3 DESAT Detection Threshold

There are two ways to alter the DESAT detection threshold. Adjustment of RDSAT can coordinate the threshold with a particular VDS during desaturation, while insertion of RZ reduces the threshold by the Zener voltage.

The value of RDSAT can be adjusted to control the IDS DESAT current level. Below is an equation to estimate the value of RDSAT.

$$RDSAT = \frac{(V_{DESAT} - V_{DS} - V_f)}{I_{\text{chg}}}$$

Equation 5.5. RDSAT with No RI Enhancement

The value of RDSAT_E (enhanced) can be adjusted to control the IDS DESAT current level. Below is an equation to estimate the value of RDSAT_E:

Through current superposition:

$$I_{\text{RI}} = (V_{\text{DDB}} - 0.6 - V_{DESAT})/RI$$

$$I_{\text{RDSAT}} = I_{\text{chg}} + I_{\text{RI}}$$

$$RDSAT_E = (V_{DESAT} - V_{DS} - 0.6)/I_{\text{RDSAT}}$$

Equation 5.6. RDSAT_E with RI Enhancement

The effective DESAT threshold can be lowered by the addition of a Zener diode (with lower voltage than the DESAT threshold minus n diode drops) in series with RDSAT.

$$V_{DESAT_Z} = V_{DESAT} - V_Z$$

Equation 5.7. DESAT Threshold with VZ

Any of the above methods of threshold adjustment may be combined.

The two blocking diodes DDSAT1 and DDSAT2 serve to keep high voltage from the switch drain from damaging the DSAT pin of the driver device. There are two diodes here for added breakdown voltage protection while maintaining low reverse-bias capacitance.

It is very important to understand that in the case of a low-side switch drain short to the positive rail, none of the DESAT threshold adjustments will affect the blanking time or detection time as the DESAT diode will be reverse biased. Therefore, the sum of blanking time, DESAT delay, and Soft Shutdown Time must be short enough to prevent damage to the switch, even with the default detection threshold. This is also true for a high-side switch with its source shorted to the negative rail.

5.2.4 Soft Shutdown Adjustment

TSS can be adjusted by RSS. Effective soft start resistance is $R_{\text{SS}} + R_{\text{H}}$. See application note, [AN1288: External Enhancement Circuits](#), for details. When VH is pulled down by the internal soft shutdown drive, it pulls base current from Q3 which results in active pull down on the emitter of Q1, pulling the gate of the power switch low. RSS can be adjusted to increase this pull down current and reduce the soft shutdown time.

5.2.5 External Miller Clamp

The internal Si828x Miller Clamp provides additional security to the low-side switch during its off time. The addition of the external Miller Clamp enhances this behavior for the cases where the high positive dv/dt of a SiC switching node can result in a coupling current through the C_{DG} , which tends to turn the device on.

5.2.6 Recommended Protection

To help protect the SiC gate from over-voltage events, we recommend adding Schottky diodes from VSSB to the gate and from the gate to VDDB. An example of such an event is current injection via the drain-gate capacitance due to inductive kickback.

6. Turn-On Characteristics

SiC MOSFET devices have turn-on characteristics that distinguish them from silicon MOSFETs and IGBTs, and which have implications for gate drive circuits. The gate driver must drive high enough to fully turn on the device and keep it in the positive temperature region of $R_{DS(on)}$, low enough to fully turn it off and prevent noise margin issues, and quickly enough to eliminate unnecessary switching losses due to $R_{DS(on)}$.

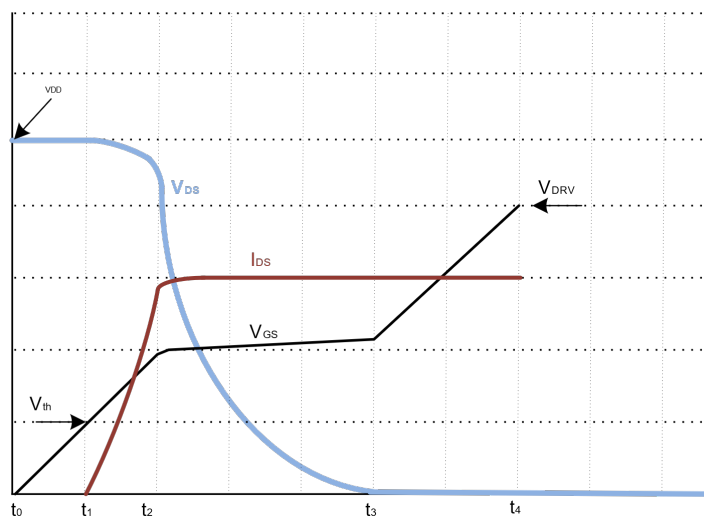


Figure 6.1. Turn-On Characteristics

6.1 Low Transconductance

Low transconductance can be seen in the soft knee of the I_D v. V_{DS} family of curves. This means that driving the device to a high drain current requires a rather large V_{GS} , in the range of 15 V to 20 V (refer to your specific switch device data sheet). If the device is operated at a low V_{GS} , the resulting high R_{DS} may result in thermal stress or device failure. Transconductance has a direct influence on several dynamic behavior characteristics that one must consider (on-resistance, gate charge [Miller plateau] and over-current [DESAT] protection). The Si828x provides high V_{GS} drive as discussed in [5.2.1 Gate Drive](#).

6.2 On Resistance

The on-resistance of a silicon carbide MOSFET has three V_{GS} -dependent components: 1) the channel resistance, which has a negative temperature coefficient and is the dominant contributor to on-resistance at lower V_{GS} , 2) JFET resistance, and 3) drift region resistance. The last two are positive temperature coefficients and dominate the on-resistance at higher V_{GS} . At lower V_{GS} , channel resistance will dominate and the on-resistance will tend to have a negative temperature coefficient at temperatures below 25 °C. At higher V_{GS} (above threshold), on-resistance temperature coefficient will always be positive. A high V_{GS} is important when operating devices in parallel to prevent uneven thermal sharing that might occur if the switches operated in the NTC region. The Si828x provides high V_{GS} drive as discussed in [5.2.1 Gate Drive](#).

6.3 Internal Gate Resistance

Internal gate resistance is inversely proportional to die area and will be higher for a SiC MOSFET than for a comparable silicon MOSFET. However, the smaller size of the SiC device results in significantly lower input capacitance and lower gate charge. A silicon device may have the same gate time constant as a comparable silicon carbide device, but the silicon gate resistance may be as much as seven times higher. The internal gate resistance limits the drive current available to charge the gate capacitance. The gate driver must have a very low output impedance, so it does not add to the internal gate resistance and limit the design range of the external gate resistances. The external BOM enhancements described in this document provide a very low gate drive output impedance as discussed in [5.2.1 Gate Drive](#).

6.4 Gate Charge and High Miller Plateau

The internal capacitances of the silicon carbide MOSFET are nonlinear. These must be charged by the driver as quickly as possible to minimize switching losses developed in the channel on-resistance. The total gate charge can be quantified and characterized to facilitate the design of the low-impedance driver.

The VGS v. gate charge curve can be modeled as three linear segments: 1) from zero gate charge to initial turn-on, 2) the Miller plateau, and 3) from the high edge of the Miller plateau to completely on. Zero gate charge does not occur at VGS = 0 V, but rather at a negative voltage, so the gate must be driven below zero voltage to totally discharge the gate. The Miller plateau is not flat as one would find with a silicon MOSFET; it has a positive slope, which means VGS will change over the charging range of this region. The Miller plateau also occurs at a higher VGS than for a silicon MOSFET. The gate driver must be able to provide maximum current drive at this VGS to overcome the plateau quickly and drive the device into saturation before conduction losses during switching can result in unnecessary power loss. Once out of the Miller plateau, the gate can again be charged quickly to its maximum. The gate drive enhancement discussed in [5.2.1 Gate Drive](#) provides maximum current at the Miller plateau VGS.

7. Switching Characteristics

SiC MOSFETs have dynamic switching behavior very similar to standard silicon MOSFETs, but SiC device characteristics impose unique gate drive requirements that must be accounted for.

7.1 Gate Drive Resistance Dampens the Gate Driver Pulse, Eliminating Excessive Ringing on the Gate Drive Signal

Due to the high slew rate of the gate drive, parasitic inductances may be a factor in SiC circuits. External gate drive resistance (as seen in [Figure 4.2 Driver Model with Three Output Pins on page 7](#)) is used to dampen the inductive effects, reducing or eliminating excess ringing on the gate drive signal. This is important, as excess ringing may result in partial turn-off or unintentional turn-on of the SiC MOSFET. The values of R_H and R_L should also be chosen to minimize shoot-through current in a half-bridge circuit by turning off the high-side switch more quickly than turning on the low-side switch (see [Figure 7.4 Lower Shoot-Through Current, \$R_H \gg R_L\$ on page 17](#)). The gate drive enhancement discussed in [5.2.1 Gate Drive](#) provides a very low output impedance, which in turn allows a greater range of R_H and R_L .

7.2 Calculating RH, RL Gate Resistors

The switching transition time depends on how quickly the total gate charge Q_g is delivered, which in turn depends on the amplitude of the gate current. External gate resistors R_H and R_L may be adjusted to optimized switching transition times t_{rise} and t_{fall} by selecting the values of the gate resistors for a desired gate current level.

$$Q_{total} = I_g \times t \text{ or } I_g = \frac{Q_{total}}{t}$$

Equation 7.1. Gate Charge, Gate Current over Transition Time

From the equation above and the information in the above figure, the gate current required to switch the power device between the ON and OFF states can be approximated:

$$I_{g_on} = \frac{Q_g}{t_{rise}}; \quad I_{g_off} = \frac{Q_g}{t_{fall}}$$

Equation 7.2. Gate Current

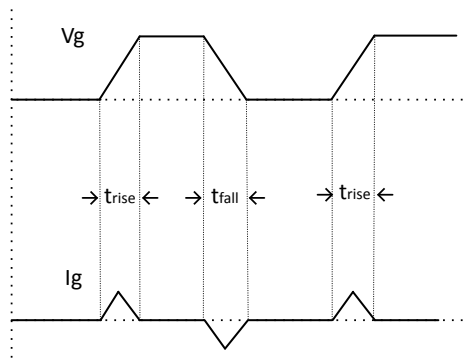


Figure 7.1. Gate Current During Switching

Notice that for the driver with three output pins (VH/VL/CLMP), the gate turn-on (I_{g_on}) and turn-off current (I_{g_off}) can be different for applications with different rise and fall time requirements. For the Si8286 driver with one output pin (VO) (see [Figure 4.1 Simple Driver Model on page 6](#)), the rise and fall times are the same because both charging and discharging currents flow through the same R_g resistor, unless there is a separate diode/resistor return path for different turn-off time.

The R_H can be calculated using Ohm's law and the driver's operating voltage V_{DDB} (V_{DRV}).

$$R_H = \frac{V_{DDB} - V_{Dshottky} - V_{BE_NPN}}{I_{g_on}} - R_{OH}$$

Equation 7.3. RH Resistor

R_{OH} is the impedance of the NPN driver in the gate drive enhancement circuit. This may be determined empirically or determined from the R_{SAT} specification (if provided) in the transistor data sheet.

The power switch turn-off process is the reverse of the turn-on phenomenon. The gate charge built up during the turn-on transition must be removed to bring the power device to a fully OFF state. The gate voltage from the ON state is equal to V_{DDB} (sustained by the gate capacitors). This voltage level needs to "discharge" to 0 V to turn off the power device.

$$R_L = \frac{V_{DDB} - V_{BE_PNP}}{I_{g_off}} - R_{OL}$$

Equation 7.4. RL Resistor

R_{OL} is the impedance of the PNP driver in the gate drive enhancement circuit. This may be determined empirically or determined from the R_{SAT} specification (if provided) in the transistor data sheet.

7.3 Coordinating RH and RL Values to Minimize Shoot-Through Current

The following figure illustrates a half-bridge power circuit with three-output-pin drivers. This type of power circuit can suffer shoot-through current (current created when both QH and QL are ON) if driven by complementary (+IN, -IN) input signals and having the same values for RH and RL.

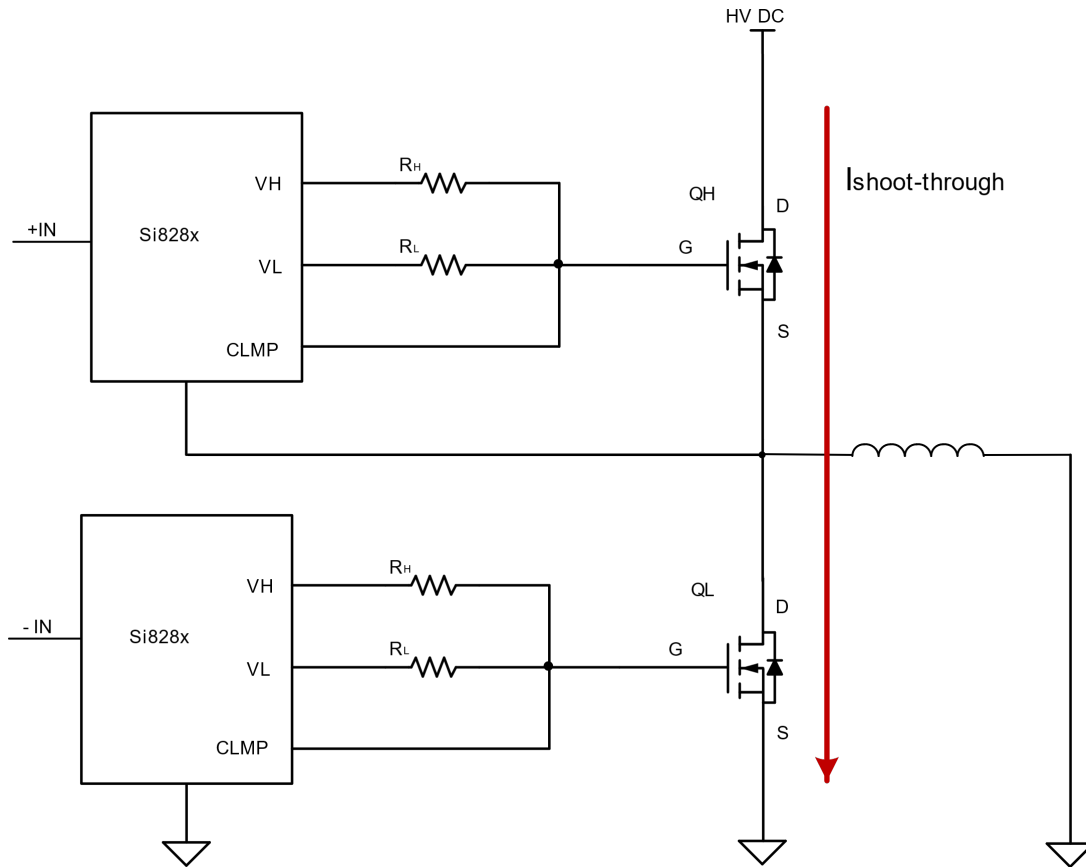


Figure 7.2. Half-Bridge Circuit with Three-Output-Pins Driver

Moreover, power devices are not ideal switches and the transition between ON and OFF states does not occur cleanly. There is a period during the switching transition when both switches are in the half-on and half-off state. This condition allows current from the HV-DC rail to flow directly through both QH and QL to ground (see figure above). Shoot-through current dissipates excessive amounts of power in the switching devices because it flows directly across the high voltage dc rail. This is part of switching loss and should be minimized for robust operation.

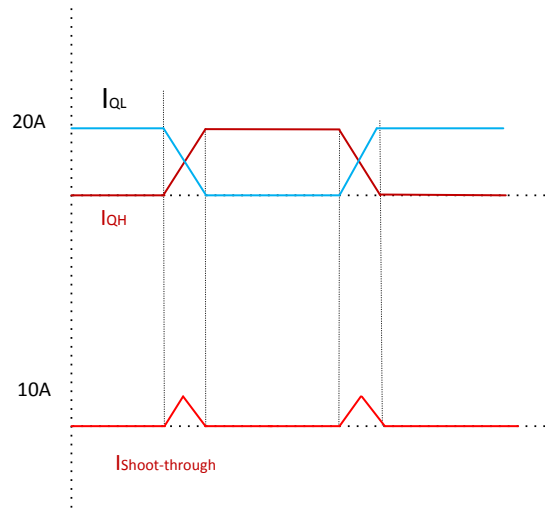


Figure 7.3. Shoot-Through Current at Switching, $R_H = R_L$

One method to minimize shoot-through current is to turn the switches on slowly and to turn them off quickly. This method ensures that one device is closer to a complete turned-off state before the other one is turned on. This method can be easily implemented with the 3- output-pin driver by having larger R_H and smaller R_L resistor values. A large R_H value reduces the charging current to the gate capacitor and lengthens the turn-on time while the smaller R_L value speeds up the turn-off time. The figure below illustrates a smaller shoot-through current using this method where $R_H \gg R_L$.

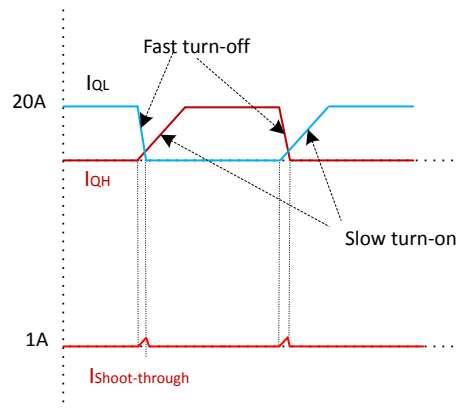


Figure 7.4. Lower Shoot-Through Current, $R_H \gg R_L$

7.4 RH, RL Power Dissipation

In [Figure 4.2 Driver Model with Three Output Pins](#) on page 7, the current flows through resistors RH and RL to charge and discharge the gate capacitors. Depending on the switching frequency, VDDB voltage level, and the total gate charge of the power switch device, the power dissipation of these gate resistors must be considered. Therefore, proper package selections are required to ensure that the resistors can handle the power dissipation appropriately. Power dissipation of the gate resistors occurs only during the turn-on and turn-off transitions.

Upon turn-on, current flows from VDDB through the R_{SAT} (saturation resistance of the NPN) and RH resistors (see figure below) to charge the gate capacitor, C_g. At the end of the turn-on transition, the voltage at the gate capacitor reached the VDDB level minus the V_{BE} of the NPN. Half of the total charging energy from VDDB is stored in the gate capacitor and the other half is dissipated on the gate resistors RH and R_{SAT}. The power dissipation on the resistor is split between R_{SAT} and RH proportionally to their resistance.

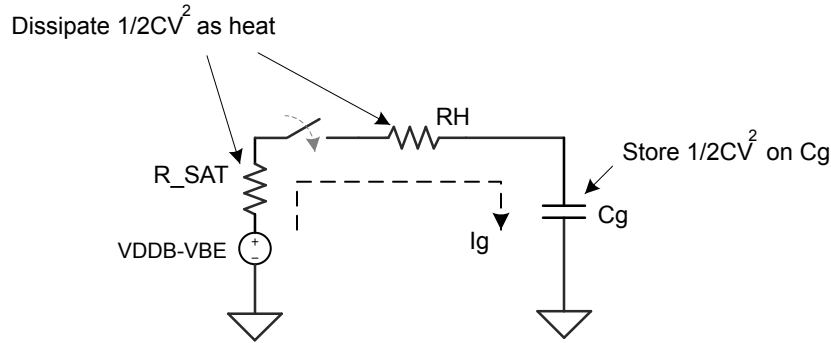


Figure 7.5. R_gTurn-On Power Dissipation

$$P_{RH} = \frac{1}{2}fC_g(V_{DDB} - V_{schottky} - V_{BE})^2 \left\{ \frac{RH}{R_{SAT} + RH} \right\} = \frac{1}{2}fQ_g(V_{DDB} - V_{schottky} - V_{BE}) \left\{ \frac{RH}{R_{SAT} + RH} \right\}$$

Equation 7.6. RH Power Dissipation

Upon turn off, current flows from C_g through RL and R_{SAT} to ground (see figure below) to discharge the C_g stored energy (from turn-on). The voltage on C_g begins at VDDB - V_{BE} voltage level and ends at ground voltage level, and all stored capacitive energy is dissipated on resistors RL and R_{SAT}.

$$P_{RL} = \frac{1}{2}fQ_g(V_{DDB} - V_{BE}) \left\{ \frac{RL}{R_{SAT} + RL} \right\}$$

Equation 7.7. RL Power Dissipation

8. DSAT Fault Indication and Fault Reset

Right after the DSAT condition is detected ($V_{DSAT} > 7V$), the fault indication is propagated toward the FLTb pin and arrives after the t_{DESAT} to FLTb delay (see the figure below). The DESAT fault condition can be cleared by bringing the RSTb pin low for a minimum duration of 350 ns. Notice that the RSTb input is level-sensitive reset logic and keeping RSTb low continues to reset the driver output. The recommended fault condition clearing sequence is to bring the input signals at the IN pins to low logic level and then pulse the RSTb pin low for a minimum duration of 50 ns. The driver is now ready to drive the power switch with input signals from the IN pins.

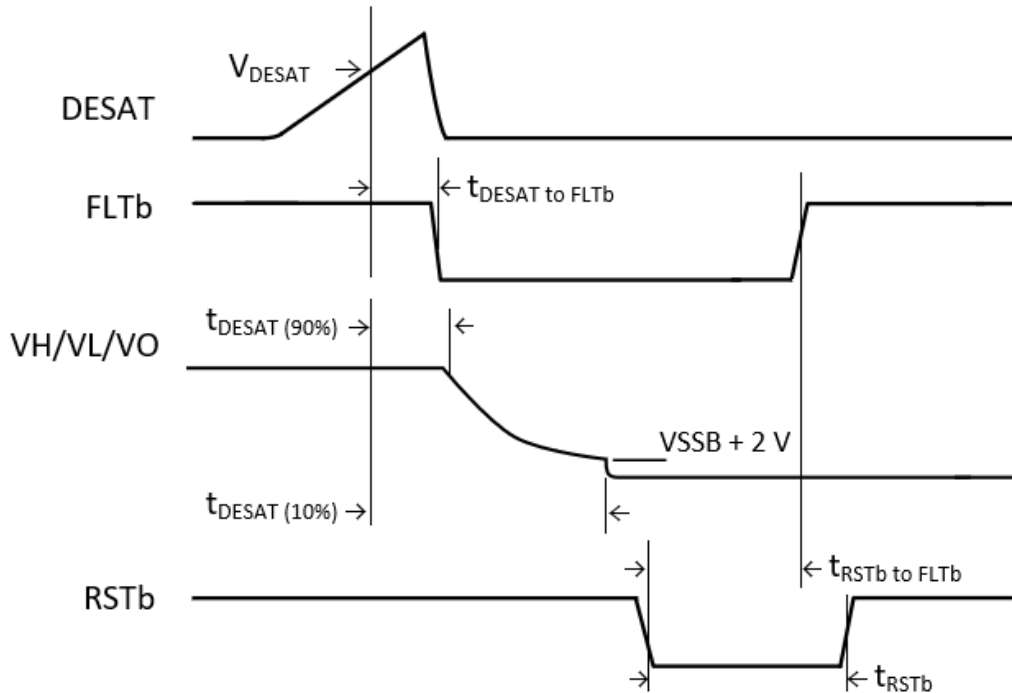


Figure 8.1. DESAT and Soft Shutdown

9. UVLO

The undervoltage lockout (UVLO) feature monitors the output supply and ensures that the device only drives the gate if there is sufficient voltage to achieve the desired V_{GS} for complete turn-on. If the value of the output supply $V_{DDB-VMID}$ drops below $V_{DDB_{UV-}}$, the device enters UVLO mode. VL will be driven low until $V_{DDB-VMID}$ rises above $V_{DDB_{UV+}}$.

A UVLO condition will result in the FLTb pin being driven low. FLTb is an open-drain type output. Once the UVLO condition is cleared on the driver side of the device, the FLTb pin is released. A pull-up resistor takes the pin high. The current version of the Si828x family has added UVLO threshold options at 13 V and 15 V to provide for fault indication when the output supply falls below values supporting SiC devices' optimal V_{GS} turn-on voltage.

10. Conclusion

Silicon carbide devices have some unique characteristics and these impact SiC MOSFET switch driver requirements. These have been discussed in detail. Gate drive models have been presented. The Si828x isolated gate driver has standard features which, when modified with external BOM enhancements, will optimally drive SiC MOSFET switches in the most demanding applications. These enhancements and their behaviors are described in application note, "[AN1288: Si828x External Enhancement Circuits](#)".

11. References

- ["Silicon carbide MOSFETs: Superior switching technology for power electronics applications"](#), Electronic Products.
- ["Application Considerations for Silicon Carbide MOSFETs"](#), Cree Inc.
- Skyworks application note, ["AN1167: Safety Considerations for Skyworks Series Capacitor Isolators"](#).
- Skyworks application note, ["AN583: Safety Considerations and Layout Recommendations for Digital Isolators"](#).
- Skyworks application note, ["AN1288: Si828x External Enhancement Circuits"](#).



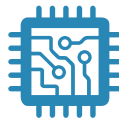
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